



PowerPC G5

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Introduction

Key Features

- 64-bit architecture, capable of addressing vast amounts of memory
- Native support for 32-bit applications
- Frontside bus up to 1.25GHz, allowing a constant flow of data in and out of the processor
- Dual independent frontside buses in dual processor systems
- Superscalar execution core supporting up to 215 in-flight instructions
- Velocity Engine for accelerated single-instruction, multiple-data (SIMD) processing
- Two floating-point units for high-speed double-precision calculations
- Advanced three-component branch prediction logic to increase processing efficiency

In June 2003, Apple introduced the PowerPC G5, marking the arrival of a 64-bit processor architecture to the personal computer market. This revolutionary processor made its debut in the Power Mac G5, enabling computer users to tackle projects never before possible on a desktop system—and blaze through their work faster than ever. With the introduction of the new Power Mac G5 and Xserve G5, the PowerPC G5 takes on even more demanding work, accelerating a wide range of intensive desktop, server, and High Performance Computing (HPC) applications.

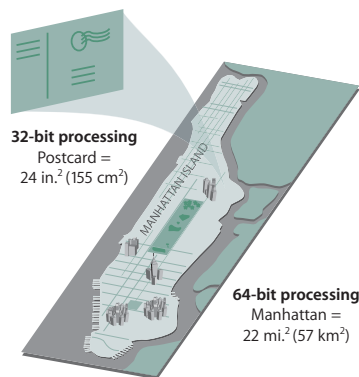
The PowerPC G5 is the product of a long-standing partnership between Apple and IBM, two companies committed to innovation and customer-driven solutions. In 1991, they co-created a PowerPC architecture that could support both 32-bit and 64-bit instructions. Leveraging this design, Apple went on to bring 32-bit RISC processing to desktop and portable computers, while IBM focused on developing 64-bit processors for enterprise servers. The PowerPC G5 represents a convergence of these efforts: Its design is based on the PowerPC instruction set, as well as the award-winning IBM POWER Architecture.

Now available in Apple desktop computers and Apple servers, the PowerPC G5 boasts a next-generation architecture built for speed and massively parallel operations:

- The ability to address vast amounts of memory provides fast data access, boosting performance for 2D and 3D imaging, video rendering tasks, and transaction-intensive workgroup and Internet services.
- A dual-channel frontside bus at up to 1.25 gigahertz provides high bandwidth to and from the rest of the system, allowing large numbers of tasks to run concurrently.
- Fast L1 and L2 caches, group instruction dispatching, deep queues, and three-stage branch prediction logic increase processing efficiencies.
- A superscalar execution core with 12 functional units improves performance by executing multiple instructions per cycle in parallel.
- An optimized 128-bit Velocity Engine cranks through image editing tasks, high-definition video transitions, media encoding, and complex scientific analysis.
- Two double-precision floating-point units accelerate 64-bit calculations for 3D visualization, research simulations, and multitrack audio creation.

The results are phenomenal. The PowerPC G5 boasts across-the-board performance enhancements that enable media applications and server transactions to run up to twice as fast. Best of all, existing 32-bit applications run natively on the PowerPC G5, so the transition to 64-bit processing is absolutely seamless. This enormous computing power is available on Apple systems today.

64-Bit Processor Technology



4.3 billion times bigger

To grasp the enormous leap from 32-bit to 64-bit processing, imagine equating the range of numbers a processor can express with a two-dimensional area. A 32-bit processor can express a range of integers equal to the size of a postcard, while a 64-bit processor can express a range of integers larger than the island of Manhattan.

The 64-bit PowerPC G5 is all about performance. With 64-bit-wide data paths and registers, it represents an exponential leap in processing power over traditional 32-bit processors. The groundbreaking PowerPC G5 can address vast amounts of main memory, while completing multiple 64-bit integer and double-precision floating-point calculations in every clock cycle.

An Exponential Leap in Computing Power

The labels “32-bit” and “64-bit” characterize the width of a microprocessor’s data stream, which is a function of the sizes of its registers and the internal data paths that feed the registers. A 64-bit processor moves data and instructions along 64-bit-wide data paths—compared with the 32-bit-wide paths on 32-bit processors, such as Intel’s Pentium 4 and Xeon. In addition, 64-bit processors have wide registers that can store extremely large or extremely precise 64-bit numbers.

The leap from 32-bit to 64-bit processing represents an exponential advance in computing power. With 32-bit registers, a processor has a dynamic range of 2^{32} , or 4.3 billion—which means it can express integers from 0 to 4.3 billion. With 64-bit registers, the dynamic range catapults to 2^{64} , or 18 billion billion—4.3 billion times larger than the range of a 32-bit processor. This means that computations involving very large integers or very precise numbers with extended decimals can be completed in one pass through the functional units, rather than several passes.

Vast Amounts of Addressable Memory

The move to 64-bit processing results in a similarly dramatic leap in the amount of memory supported. Computers keep track of data stored in memory using memory addresses. A memory address is a special kind of integer, which points to one byte in memory. Since memory addresses are computed in 64-bit registers capable of expressing 18 billion billion integers, the PowerPC G5 can theoretically address 18 exabytes (18 billion billion bytes) of virtual memory.

In practice, memory addressing is defined by the physical address space of the processor. The PowerPC G5, with 42 bits of physical address space, supports a colossal 2^{42} bytes, or 4 terabytes, of system memory. Although it’s not currently feasible to purchase 4 terabytes of RAM, the advanced architecture of this processor allows for plenty of growth in the future.

Very large quantities of RAM enable a desktop system to contain a gigantic 3D model, a complex scientific simulation, or an entire database in main memory. When data is stored in memory, the processor can access it 40 times faster than from the hard drive, drastically reducing the time to access and manipulate data. For server tasks that treat each user connection as a separate process, such as web hosting or database publishing, each process can access its own large memory space, allowing the system to cache relevant data for each user—for virtually instant response.

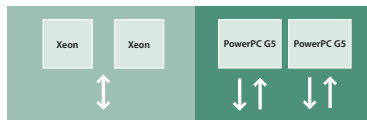
Multiple High-Precision Calculations

With 64-bit-wide data paths and registers, the PowerPC G5 can execute multiple instructions on 64 bits of data—including huge integer calculations and double-precision floating-point mathematics—in every clock cycle. In contrast, a 32-bit processor has to split up any data larger than 32 bits and process it in multiple passes. This leap in performance, from 32-bit to 64-bit processing, brings previously unmanageable tasks into the realm of practicality, facilitating highly accurate calculations required for scientific analysis, 3D effects, and video encoding. For example, a 3D model that would take all day and night to render on a 32-bit system can be finished by noon of the same day on a PowerPC G5-based system.

Next-Generation PowerPC Architecture

The PowerPC G5 is a highly parallel implementation of the PowerPC architecture, capable of handling large numbers of tasks at the same time. It's based on the execution core of the industry-leading IBM POWER Architecture that drives IBM's top-of-the-line enterprise servers. Apple collaborated with IBM to leverage this superscalar, superpipelined design for the next generation of personal computers and entry-level servers. The development of the PowerPC G5 builds on previous PowerPC designs, combining an optimized Velocity Engine unit, two double-precision floating-point units, advanced branch prediction logic, and a high-bandwidth frontside bus to support up to 215 simultaneous in-flight instructions.

Because the PowerPC instruction set was designed from the beginning to handle both 32-bit and 64-bit code, existing 32-bit applications run natively on PowerPC G5-based computers and servers. No software modification or optimization is required, and there's no need for emulation or translation software. In fact, most 32-bit applications run dramatically faster on the PowerPC G5.



Industry's fastest frontside bus

The dual-channel frontside bus allows data to travel to and from the PowerPC G5 processor at the same time. Each PowerPC G5 has its own dedicated interface to maximize throughput—compared with dual Xeon-based systems, in which the processors must share a single bus.

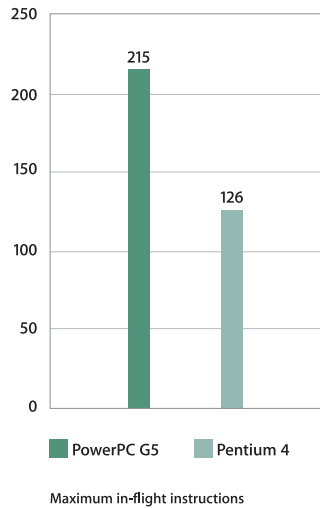
Up to 1.25GHz Frontside Bus

The performance advantages of the PowerPC G5 begin with an innovative Double Data Rate (DDR) frontside bus that speeds up communication between the processor and the memory controller. Unlike conventional processor interfaces, which carry data in only one direction at a time, this dual-channel frontside bus has two 32-bit point-to-point links (64 bits total): One link travels into the processor and another travels from the processor, which means no wait time while the processor and the system controller negotiate which will use the bus or while the bus switches direction. This elastic interface self-tunes during startup for optimal signal quality.

On a 2.5GHz PowerPC G5, the frontside bus operates at 1.25GHz for a total theoretical bandwidth of up to 10GB per second per processor. Dual PowerPC G5 systems get twice the bandwidth (20GB per second), because each processor has a dedicated frontside bus.

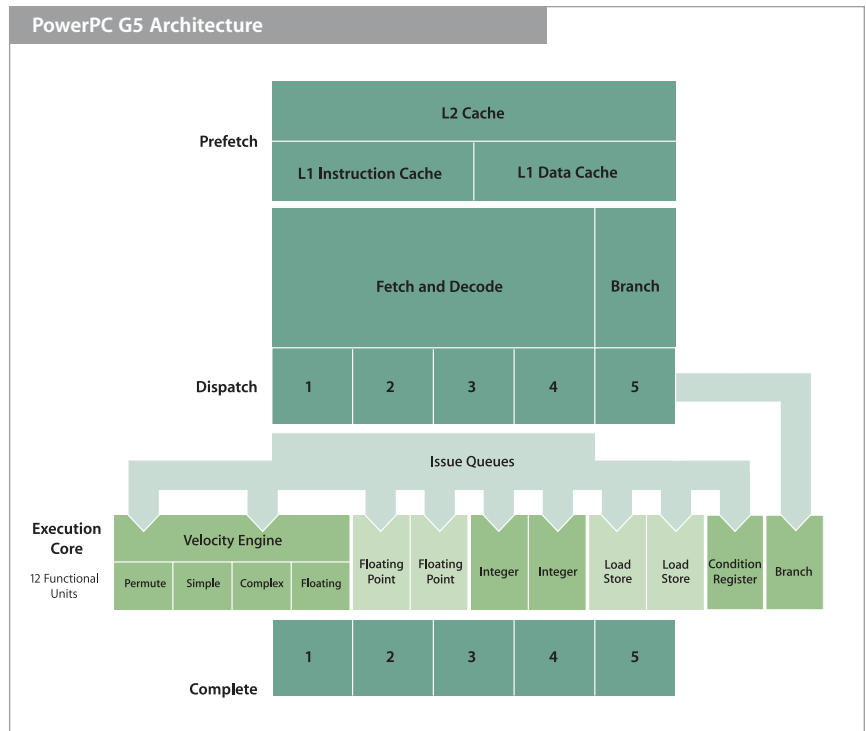
Fast Access to Data and Instructions

The PowerPC G5 features processing innovations that optimize the flow of data and instructions—making it ideal for streaming media, editing HD video, rendering 3D effects, serving databases, and hosting web applications, as well as for compute-intensive simulations and scientific analysis. Large caches and instruction preparation in the processor maximize performance as instructions are dispatched into the execution core and data is loaded into the registers.



Up to 215 in-flight instructions

A wide instruction window with 12 discrete processing units enables the PowerPC G5 to contain up to 215 in-flight instructions simultaneously—71 percent more than the 126 instructions in a Pentium 4.



Prefetch

Prefetching improves processor performance by retrieving and caching data and instructions before they’re demanded by the processor, ensuring optimal utilization of each processor cycle. The PowerPC G5 anticipates the need for data and instructions and prefetches them into its large L1 and L2 caches. To protect the integrity of data and instructions, L1 cache is parity-protected and L2 cache is protected using Error Correction Code (ECC) logic.

Fetch and decode

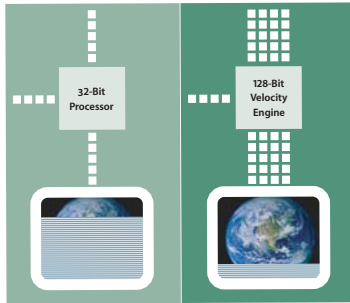
A low-latency 512K L2 cache provides fast access to data and instructions—at rates up to 64GB per second. Instructions are fetched from the L2 cache into a direct-mapped 64K L1 instruction cache. At the same time, 32K of write-through, two-way associative L1 data cache can fetch up to eight active data streams simultaneously.

Up to eight instructions per clock cycle are fetched from the L1 instruction cache for decoding. Decoding divides each instruction into smaller suboperations, giving the processor more freedom to schedule execution of code in parallel.

Group formation and dispatch

Before instructions are dispatched into the functional units, they are arranged, in program order, into groups of up to five. The PowerPC G5 dispatches these packaged groups to the queues in the execution core, where they are broken into individual instructions for out-of-order processing. When operations on the data are complete, the PowerPC G5 recombines the instructions into the original groups of five.

This grouping scheme enables the PowerPC G5 to track—and keep organized—an unusually large number of instructions with greater efficiency. By tracking groups rather than individual instructions, it can manage up to 100 instructions within the core simultaneously, in addition to 100-plus instructions in the various fetch, decode, and queue stages, for a total of 215 in-flight instructions.



The Velocity Engine can manipulate 128 bits of data per clock cycle, up to four times more than a 32-bit processor's general processing unit.

Fused multiply-add

The floating-point units in the PowerPC G5 are able to complete both a multiply operation and an add operation as part of the same machine instruction, thereby accelerating matrix multiplication, vector dot products, and other scientific computations. This instruction is referred to as fused multiply-add, or "fmadd," and is considered a basic building block for data-intensive floating-point computation.

The following computation can be completed by a fused multiply-add instruction in one pass through either of the two floating-point units in the G5:

$$T = (a * b) + c$$

On other processors, two instructions are required. The first is a multiply instruction:

$$U = (a * b)$$

The product "U" would be used later by a second instruction, an addition, to complete the computation:

$$V = U + c$$

Thus, in processors with comparable clock speeds, the computation of "(a * b) + c" can be completed twice as fast using fused multiply-add.

What's more, on the G5, round-off occurs just once in the computation of "T," while on other processors, round-off occurs twice, both in the computation of "U" and in the computation of "V," so fused multiply-add can deliver a more accurate result.

Issue queues

The PowerPC G5 includes eight deep issue queues that maximize the utilization of each functional unit. Individual instructions are issued to the appropriate functional unit at up to ten instructions per clock cycle. Each functional unit has a dedicated issue queue, where multiple instructions are sequenced for processing.

Superscalar Execution Core

At the heart of the PowerPC G5 is a superscalar execution core, composed of 12 functional units that execute different types of instructions concurrently for massive data throughput.

128-bit Velocity Engine

This powerful 128-bit vector processing unit accelerates data manipulation by applying a single instruction to multiple data at the same time, known as SIMD processing. Vector processing is useful for transforming large sets of data and other computationally intensive tasks, such as manipulating 3D images, rendering a video effect, encoding live media, or encrypting data. For example, when a designer uses a filter to apply a motion blur to an image, each pixel of the image must be changed according to the same set of instructions—a highly repetitive processing task.

The Velocity Engine on the PowerPC G5 has been optimized with two independent queues. It uses the same set of 162 instructions implemented in the PowerPC G4, enabling it to accelerate existing Mac OS X applications that have been optimized for the Velocity Engine. While operating concurrently with the integer and floating-point units, the Velocity Engine also supports highly parallel internal operations—for simultaneous processing of up to 128 bits of data in four 32-bit integers, eight 16-bit integers, sixteen 8-bit integers, or four 32-bit single-precision floating-point values.

Double-precision floating-point units

Today's powerful applications demand both precision and performance. That's why the PowerPC G5 has twice the double-precision floating-point hardware of the PowerPC G4, enabling it to complete at least two 64-bit mathematical calculations per clock cycle. In fact, each of its two floating-point units can perform both an add and a multiply with a single instruction, as well as full-precision square root calculations, for dramatic acceleration of complex computations.

Double-precision floating-point math is critical in research simulations and in many of the applications used to manipulate or render 3D graphics and video content. Weather prediction is one example of a highly iterative computing task that requires floating-point math. Large-scale models simulate weather patterns over time by measuring multiple influences, such as atmospheric pressure and airflow, at various instants and recalculating the model every minute. The floating-point capabilities of the PowerPC G5 provide the precision and performance to deliver accurate results within a useful timeframe.

Integer units

Integer units perform basic arithmetic and logic operations—such as add, subtract, multiply, and compare—which are used in virtually all computer functions, as well as in imaging, video, and audio applications. The PowerPC G5 has two integer units capable of both simple and complex instructions involving 32-bit or 64-bit data. What's more, they take full advantage of the processor's 64-bit registers and data paths to complete simple 64-bit integer calculations in a single clock cycle.



Machined for math

Virginia Tech chose the PowerPC G5 as the engine for its supercomputer facility, ranked third most powerful in the world.* This supercomputer will be used to conduct multidisciplinary work on such topics as nanoelectronics, aerodynamics, and the molecular modeling of proteins, and will enable researchers to simulate complex models in days rather than years.

Dedicated register files

To provide fast access to data, the PowerPC G5 is equipped with three sets of high-performance, low-latency register files: one containing 64-bit registers for integer calculations, one with 64-bit registers for floating-point calculations, and one with 128-bit registers for vector calculations. Each register file holds 32 registers for architected values, as well as 48 rename, or proxy, registers.

Load/store units

Load/store units perform memory-access operations, loading data into the registers of each functional unit and, after processing, storing the new data in L1 cache, L2 cache, or main memory as appropriate. With two load/store units, the PowerPC G5 is able to keep its wide instruction window filled with data for maximum processing efficiency.

Since the PowerPC G5 is capable of handling more than 200 in-flight operations, it needs a robust storage mechanism for the data associated with those instructions. While the instructions are being scheduled in the core, the load/store units load the associated data from L1 cache into the data registers behind the units that will be processing the data. To improve processing efficiency, the PowerPC G5 features a large number of rename registers that act as proxies, or placeholders, until the appropriate data arrives for execution. The instruction is held in queue, allowing other operations to take place until the actual data is loaded into the registers.

Condition register unit

When instructions have finished executing, they have the option to store information about their outcome in the processor's 32-bit condition register for future reference. The condition register can hold up to eight condition codes, which describe the outcome of eight different instructions. To improve the flow of data throughout the execution core, subsequent operations—such as branch instructions—can consult the condition register for the results of earlier operations.

The condition register unit performs logical operations related to the condition register. Programmers can manipulate and compare condition codes using a collection of PowerPC instructions, which are executed in this special functional unit. These comparisons are normally handled by an integer unit in other processors. With a dedicated functional unit for condition code comparisons, the PowerPC G5 effectively reduces the workload of its two integer units.

Branch prediction unit

Advanced processors use branch prediction and speculative instruction execution to keep processing resources constantly in use. A branch is a question in the processing queue: Which instruction should go next? Branch prediction anticipates the answer; and speculative execution schedules that instruction. If the prediction is correct, the processor works more efficiently, because the instruction has executed before it is required. If the prediction is incorrect, the processor must clear the unneeded branch, as well as any related data and instructions, resulting in an empty space called a pipeline bubble. Pipeline bubbles reduce performance as the processor marks time waiting for the next instruction.

The branch prediction unit on the PowerPC G5 uses innovative three-component logic to reduce pipeline bubbles and maximize processor efficiency. The success or failure of each prediction is captured in three large 16K branch history tables—local, global, and selector—that are used to improve the accuracy of future branch predictions.

Local branch prediction takes place as individual instructions are fetched into the processor and the types of branches are recorded in the local branch history table. Global branch prediction occurs at the same time: Branches are identified in their processing context, relating to preceding and subsequent operations; and the results are recorded in the global branch history table. The third, "selector" history table identifies which prediction type, local or global, was more accurate in predicting the outcome of each branch. This dynamic local/global/selector branch history scheme can predict branch processes with a high degree of accuracy, allowing the PowerPC G5 to efficiently use every processing cycle.

Designed for Symmetric Multiprocessing

Dual processors provide the high-density power and scalability required by applications in audio and video production; rendering, encoding, and compression farms; and research and computational clustering environments. Traditional server tasks also benefit from the increased bandwidth provided by multiprocessing, as many assorted transactions that use network file services, serve web pages, access databases, and authenticate users can be processed concurrently.

The PowerPC G5 is designed for symmetric multiprocessing. Dual independent frontside buses allow each processor to handle its own tasks at maximum speed with minimal interruption. At the same time, this high-performance bus interface enables each processor to discover and access data in the other processor's caches, a technique called intervention, or snooping. Cache intervention guarantees cache coherency, which ensures that the processor always fetches the correct data, even if it has been modified and is stored in the cache of the other processor.

For maximum efficiency, dual PowerPC G5 systems work with the operating system to schedule priorities. With sophisticated multiprocessing capabilities built in, Mac OS X and Mac OS X Server dynamically manage multiple processing tasks across the two processors. This allows dual PowerPC G5 systems to accomplish up to twice as much as a single-processor system in the same amount of time, without requiring any special optimization of the application.

64-Bit Capabilities in Mac OS X



Mac OS X v10.3 “Panther”

With a robust and open UNIX-based foundation, Mac OS X and Mac OS X Server offer breakthroughs in innovation, ease of use, and reliability.

Mac OS X is a robust UNIX-based operating system that includes full support for preemptive multitasking with protected memory and symmetric multiprocessing. Apple has written Mac OS X version 10.3 and Mac OS X Server version 10.3 to leverage the 64-bit features of the PowerPC G5 architecture, providing advanced computation power and more main memory for industry-leading application performance.

While Mac OS X and the PowerPC G5 are the perfect platform for next-generation creative, scientific, and networking applications, they also run today’s 32-bit applications natively. There’s no need for emulation software or additional investment in applications, allowing users to upgrade their workflows to G5 hardware without interruption. What’s more, unmodified application code takes immediate advantage of faster processor clock speeds. Applications optimized for the Velocity Engine on the PowerPC G4 use the same instruction set on the more efficient G5 processor, resulting in faster vector operations.

Performance gains are most dramatic when applications—particularly compute-intensive applications—are recompiled for the PowerPC G5. Developers can use Apple’s Xcode tools to optimize their software for maximum performance on Apple’s G5-based systems.

Updated Kernel and Numerical Libraries

On all Apple systems, Mac OS X and Mac OS X Server feature a high-performance 64-bit file system that supports HFS+ (and HFS+ journaled) file systems up to 16TB, so users can create very large, single file systems for massive databases, image archives, and digital video storage. In addition, Apple has optimized version 10.3 for the PowerPC G5 architecture, enabling current 32-bit applications to benefit immediately from the key advances of 64-bit processing. On PowerPC G5-based systems, Mac OS X can utilize the processor’s 64-bit instructions and registers.

Mac OS X version 10.3 can also address the 4TB of physical memory supported by the PowerPC G5. To ensure binary compatibility with existing 32-bit applications, Mac OS X manages access to the 64-bit physical memory space using a 32-bit virtual memory manager. This enables each Mac OS X application to access 4GB of address space, allowing multiple memory-intensive applications to run concurrently. For improved performance, data-intensive applications that require more than 4GB of memory can map pages of memory using the built-in mmap function.

PowerPC G5-optimized libraries

To optimize application performance on the PowerPC G5, Mac OS X v10.3 includes new math, vector, and image processing routines:

- Double-precision transcendental functions (libm)
- Vectorized transcendental functions (vMathLib)
- 128-bit integer math (vBigNum)
- Basic Linear Algebra Subprograms (BLAS)
- Linear Algebra Package (LAPACK)
- Vectorized digital signal processing (vDSP)
- Vector image processing (vImage)

Mac OS X v10.3 includes a collection of highly optimized libraries that take advantage of new and faster math functions supported by the 64-bit PowerPC G5. These advanced math and vector libraries use the best-possible functionality for a specific PowerPC processor. Existing applications that use the built-in math libraries will benefit—without modification—from these enhancements. For example, applications use the Apple library routine for the square root function rather than calculating it themselves. On G4 and G3 systems, the math library computes the square root using a software algorithm, while on G5 systems, it uses the much more efficient hardware instruction.



**Integrated development for
Mac OS X and Mac OS X Server**

Apple's robust Xcode tools make it easy to build high-performance applications for the PowerPC G5 processor.

Software Development for the PowerPC G5

Xcode, Apple's development toolset, makes it easy to optimize applications for the massively parallel execution core of the PowerPC G5. An enhanced version of GCC (GNU Compiler Collection) incorporates the machine model for the PowerPC G5, taking full advantage of the PowerPC instruction grouping and supporting the enhanced math hardware functions. By recompiling with Xcode and the GCC 3.3 compiler, developers can get improved code generation that keeps the processor's integer and floating-point units constantly fed with instructions.

GCC 3.3 generates PowerPC G5-optimized code that also executes efficiently on G4 and G3 systems. This allows developers to build and qualify a single version of their applications for both 32-bit and 64-bit PowerPC-based systems. In fact, Mac OS X Panther itself was completely recompiled using GCC 3.3 to achieve the best performance possible from the PowerPC G5.

For advanced performance optimization, Xcode includes Computer Hardware Understanding Development (CHUD) tools. These powerful tools measure and evaluate performance, identifying specific areas of an application that can benefit significantly from the capabilities of the PowerPC G5. For example, the MONster tool provides direct access to integrated performance counters on the G5, which test the efficiency of application code by measuring its impact on the processor.

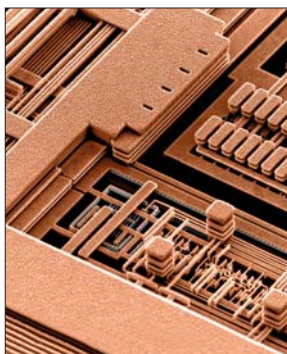
For more information about development resources for the PowerPC G5 processor, see developer.apple.com.

State-of-the-Art IBM Process Technology



Industry-leading process technology

IBM is a worldwide leader in semiconductor process technologies. The PowerPC G5 is fabricated in its \$3 billion, state-of-the-art facility in East Fishkill, New York.



Copper interconnects improve conductivity and boost processor performance.

The PowerPC G5 is fabricated in IBM's state-of-the-art facility in East Fishkill, New York. With industry-leading build, assembly, and test technology, IBM uses a 90-nanometer process with more than 58 million transistors and ten layers of copper interconnects.

To get electronics so small requires miniaturization breakthroughs, and IBM's long-standing dedication to scientific research has made these advances possible. For instance, the company began researching copper as an interconnect method over 25 years ago, but the technique didn't become practical until recently. IBM's cutting-edge process results in a small chip that can run at high clock speeds, while drawing less power and producing less heat.

Anatomy of a Processor

A microprocessor makes logic decisions based on whether its transistors are holding a charge—that is, whether they are “on” or “off.” Each transistor on the PowerPC G5 is just .00000009 meter (90 nanometers) wide, built on a layer of silicon on insulator (SOI). SOI refers to the placement of a thin layer of insulator between transistors and bulk silicon. When transistors are built on this SOI layer, their capacitance, or the tendency to store a residual electrical charge, is reduced—which results in faster operation.

The smaller the transistors, the more difficult it is to wire them together. For over 30 years, the semiconductor industry relied on aluminum wiring to connect transistors. But as semiconductors get smaller, requiring thinner and narrower connections, aluminum increasingly resists the flow of electricity and becomes harder to use. And at such small sizes, resisting electrons may even jump wires, which can turn nearby transistors on and off at random.

The PowerPC G5 uses copper interconnects to transmit electrical signals faster and more reliably than aluminum can. Its 58 million transistors are connected by over 400 meters of copper wire that is less than 1/1000 the width of a strand of human hair. These ultrathin paths allow the electrons to complete a sequence in less time, because they don't need to travel as far.

To improve conductivity further, IBM developed an additive-copper, dual-damascene wiring process as a replacement for the conventional subtractive-aluminum process. The damascene method isn't new; swords made in Damascus, Syria, over 2500 years ago were forged with this process. Ages later, the semiconductor industry began using a much evolved damascene process for copper circuit boards, but IBM was the first company to discover a method for using copper in chip wiring. The result is a 40 percent gain in conductivity and faster processor operation.

Technical Specifications

64-bit PowerPC processor architecture

- Virtual address range: 64 bits, or 18 exabytes
- Physical address range: 42 bits, or 4 terabytes
- 64-bit data paths and registers
- Native support for 32-bit application code
- 64K L1 instruction cache; 32K L1 data cache, parity-protected
- 512K internal L2 cache, ECC-protected
- Microcoded instructions for up to four internal operations per instruction
- Support for fetching up to eight instructions per cycle
- Hardware-initiated instruction prefetching from L2 cache
- Hardware- or software-initiated data stream prefetching; support for up to eight active streams

Frontside bus

- Frequency: Double Data Rate (DDR) running at up to 1.25GHz
- Width: 64-bit dual-channel

Wide execution core

- Support for up to 215 in-flight instructions
- In-order dispatch of up to five operations into distributed issue queue structure
- Simultaneous issue of up to ten out-of-order operations:
 - One Velocity Engine permute operation
 - One Velocity Engine arithmetic logic operation
 - Two floating-point operations
 - Two fixed-point register-to-register operations
 - Two load or store operations
 - One condition register operation
 - One branch operation
- Out-of-order and speculative issue of load operations
- Dual-pipeline 128-bit Velocity Engine for single-instruction, multiple-data (SIMD) processing
- Two independent floating-point units for double-precision calculations
- Three register files, each holding 32 architected values and 48 rename registers:
 - One general-purpose register file to contain 64-bit registers for integer calculations
 - One floating-point register file to contain 64-bit registers for floating-point calculations
 - One vector register file to contain 128-bit registers for vector calculations
- One 32-bit condition register containing up to eight condition codes

Three-component branch prediction logic

- Speculative superscalar inner core organization
- Fast, selective flush of incorrect speculative instructions and results
- Prediction of up to two branches per cycle
- Support for up to 16 predicted branches in flight
- Prediction hints added to branch instructions
- Prediction support for branch direction and branch addresses

Physical specifications

- 58 million transistors
- 90-nanometer, silicon-on-insulator (SOI) process
- Die size: 66 square millimeters

For More Information

For more information about the PowerPC G5 processor, visit www.apple.com/g5processor.

**Third most powerful* based on TOP500 List of Supercomputer Sites, November 2003.

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